

I CLAIM:

1. For testing semiconductor devices, a digital testing system comprising:
  - pattern memory for storing test vectors adapted for performing digital tests;
  - a digital test engine for implementing test vectors of the pattern memory, whereby digital inputs are provided to a device under test (DUT) and digital DUT outputs are captured, thereby testing the operability of the DUT.
2. A digital testing system according to claim 1 further comprising:
  - a multiplexer for interfacing the DUT with automatic test equipment (ATE); and
  - ATE operably connected to perform testing on the DUT.
3. A digital testing system according to claim 1 wherein the digital testing system further comprises a testing module.
4. A digital testing system according to claim 1 configured to perform mixed signal testing.
5. A digital testing system according to claim 1 configured to perform scan testing.

6. A digital testing system according to claim 1 configured to perform functionality testing.
7. A digital testing system according to claim 3 wherein the testing module comprises a hardware device.
8. A digital testing system according to claim 3 wherein the testing module comprises firmware.
9. A digital testing system for adding digital test capability to an automatic test equipment (ATE) platform, the system comprising;
  - automatic test equipment (ATE) adapted for performing analog testing of a device under test (DUT); and
  - a testing module further comprising pattern memory, a test engine, and a multiplexer, for performing digital testing on the DUT.
10. A digital testing system according to claim 9 wherein the testing module further comprises DDR SRAM.
11. A digital testing system according to claim 9 wherein the testing module further comprises an FPGA.

12. A digital testing system according to claim 9 wherein the testing module further comprises a high speed bus.
13. A digital testing system according to claim 9 configured to perform scan mixed signal device testing.
14. A digital testing system according to claim 9 configured to perform scan testing.
15. A digital testing system according to claim 9 configured to perform functionality testing.
16. A method for digital testing of a semiconductor device under test (DUT) positioned in a socket on a device interface board (DIB), the method comprising the steps of:
  - storing test vectors for performing tests in machine-readable memory;
  - using the test vectors, providing digital inputs to the DUT and capturing and comparing digital DUT outputs, thereby determining the operability of the DUT.
17. A method according to claim 16 further comprising the step of interfacing the DUT with automatic test equipment (ATE).

18. A method according to claim 16 further comprising the step of using automatic test equipment (ATE) for testing analog properties of the DUT.
19. A method according to claim 16 wherein determining the operability of the DUT further comprises the step of scan testing.
20. A method according to claim 16 wherein determining the operability of the DUT further comprises the step of functionality testing.
21. A method according to claim 16 wherein determining the operability of the DUT further comprises the step of mixed signal testing.